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REMARK/DISCUSSION OF ISSUES

In the NonFinal Office Action, Examiner Reis rejected pending claims 1-8 and 12-16 on various grounds. The Applicant responds to each rejection as subsequently recited herein, and respectfully requests reconsideration and further examination of the present application under 37 CFR § 1.112:

- A. Examiner Reis rejected pending claims 1-4, 6-8 and 12-16 under 35 U.S.C. § 103(a) over U.S. Patent No. 6,292,528 to *Wieczorek et al.* in view of U.S. Patent No. 6,420,213 to *Nakajyo et al.* and in further view of U.S. Patent No. 6,265,782 to *Yamamoto et al.*

The Applicant has thoroughly considered Examiner Reis' remarks concerning the patentability of claims 1-4, 6-8 and 12-16 over *Wieczorek* in view of *Nakajyo* and in further view of *Yamamoto*. The Applicant has also thoroughly re-read *Wieczorek* in view of *Nakajyo* and in further view of *Yamamoto*. The Applicant respectfully traverse this obviousness rejection of claims 1-4, 6-8 and 12-16, because Examiner Reis has failed to establish a *prima facie* case of obviousness as required by MPEP §2143. Specifically, Examiner Reis has failed to cite a suggestion or a motivation, in *Wieczorek*, *Nakajyo* and *Yamamoto* to modify *Wieczorek* in view of *Nakajyo* and in further view of *Yamamoto* to obtain the claimed invention as recited in independent claims 1 and 13.

Specifically, independent claim 1 recites "wherein said intermediate layer (2) contains at least two adhesives (A, B) of different consistency and spacers (5)", and independent claim 13 recites "said first intermediate layer (2) including a first spacer (5) in contact with said ceramic basic element (4) and said CMOS chip (3), a first adhesive (A1) adhered to said ceramic basic element (4) and said CMOS chip (3), and a second adhesive (B) adhered to said ceramic basic element (4) and said CMOS chip (3)". Examiner Reis correctly recognizes that *Wieczorek* teaches each limitation of claims 1 and 13 except for the aforementioned limitation of claims 1 and 13, that *Nakajyo* discloses the aforementioned limitation of claims 1 and 13, and that *Yamamoto* fails to teach or suggest the aforementioned limitation of claims 1 and 13. Examiner Reis therefore asserts that it would have been obvious to one of ordinary

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The basis for Examiner Reis' assertion is that *Nakajyo* suggests the desirability of the combination by offering adhesives 5 and 7 and stud bumpers 2 that can be placed between scintillator 11 (FIG. 1) and CMOS chip 9 (FIG. 1) of *Wieczorek* and between CMOS chip 9 and printed circuit board 15 (FIG. 1) of *Wieczorek* in order to ensure the standard flatness between scintillator 11 and CMOS chip 9 of *Wieczorek* and between CMOS chip 9 and printed circuit board 15 of *Wieczorek* to thereby minimize the stretch between electrical leads by preventing one side to be higher than the opposite side. However, Examiner Reis CAN NOT conclusively assert that an implementation of the adhesives 5 and 7 and stud bumpers

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2 of *Nakajyo* between CMOS chip 9 and bond pad 17 on printed circuit board 15 of *Wieczorek* would ensure the standard flatness between scintillator 11 and CMOS chip 9 of *Wieczorek* and between CMOS chip 9 and printed circuit board 15 of *Wieczorek* to thereby minimize the stretch between electrical leads by preventing one side to be higher than the opposite side. This is particularly true in view of the fact that neither *Wieczorek* nor *Nakajyo* describe an absolute minimum stretch and/or an absolute maximum stretch of the electrical leads between CMOS chip 9 and bond pad 17 on printed circuit board 15 that are conducive to reducing noise and susceptibility of interference as required by *Wieczorek* as correlated to a flatness of the various components. See, *Wieczorek* at column 2, line 43-54; and column 5, lines 13-16. Thus, one side being higher than the other does not guarantee a minimal stretch of electrical leads as asserted by Examiner Reis.

Moreover, the Applicant respectfully asserts that there is no motivation or suggestion to replace adhesive layers 13 and 16 with the adhesives and spacers of *Nakajyo* in view of the facts that (1) *Wieczorek* does not denounce adhesive layers 13 and 16 as being a less than perfect technique for bonding CMOS chip 9 and printed circuit board 15 with the goal of minimizing the stretch of electrical leads between CMOS chip 9 and bond pads 17, and (2) *Nakajyo* does not proclaim adhesives 5 and 7 and stud bumps 2 as the best technique for bonding elements (e.g., CMOS chip 9 and printed circuit board 15) with the goal of minimizing the stretch of electrical leads between the elements.

In summary, Examiner Reis fails to provide a suggestion or a motivation to modify *Wieczorek* in view of *Nakajyo* and *Yamamoto* as proposed by Examiner Reis, and *Wieczorek* teaches away from the modification of *Wieczorek* in view of *Nakajyo* and *Yamamoto* as proposed by Examiner Reis. Withdrawal of the rejection of independent claims 1 and 13 under §103(a) as being unpatentable over *Wieczorek* in view of *Nakajyo* and *Yamamoto* is therefore respectfully requested.

Claims 2-4, 6-8 and 12 depend from independent claim 1. Therefore, dependent claims 2-4, 6-8 and 12 include all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claims 2-4, 6-8 and 12 are allowable over *Wieczorek* in view of *Nakajyo*

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and *Yamamoto* for at least the same reason as set forth herein with respect to independent claim 1 being allowable over *Wieczorek* in view of *Nakajyo*.

Withdrawal of the rejection of dependent claims 2-4, 6-8 and 12 under U.S.C. §103(a) as being patentable over *Wieczorek* in view of *Nakajyo* and *Yamamoto* is therefore respectfully requested.

Claims 14-16 depend from independent claim 13. Therefore, dependent claims 14-16 include all of the elements and limitations of independent claim 13. It is therefore respectfully submitted by the Applicant that dependent claims 14-16 are allowable over *Wieczorek* in view of *Nakajyo* and *Yamamoto* for at least the same reason as set forth herein with respect to independent claim 13 being allowable over *Wieczorek* in view of *Nakajyo*. Withdrawal of the rejection of dependent claims 14-16 under U.S.C. §103(a) as being patentable over *Wieczorek* in view of *Nakajyo* and *Yamamoto* is therefore respectfully requested.

- B. Examiner Reis rejected pending claim 5 under 35 U.S.C. §103(a) over U.S. Patent No. 6,292,528 to *Wieczorek et al.* in view of U.S. Patent No. 6,420,213 to *Nakajyo et al.* U.S. Patent No. 6,265,782 to *Yamamoto et al.* and in further view of U.S. Patent No. 6,063,688 to *Doyle et al.*

Claim 5 depends from independent claim 1. Therefore, dependent claim 5 includes all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claim 5 is allowable over *Wieczorek*, in view of *Nakajyo* and *Yamamoto* and in further view of *Doyle* for at least the same reason as set forth herein with respect to independent claim 1 being allowable over *Wieczorek*, in view of *Nakajyo*. Withdrawal of the rejection of dependent claim 5 under U.S.C. §103(a) as being patentable over *Wieczorek*, in view of *Nakajyo* and *Yamamoto* and in further view of *Doyle* is therefore respectfully requested.

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SUMMARY

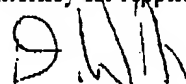
Examiner Reis' rejections of pending claims 1-8 and 12-16 have been obviated by the remarks herein supporting an allowance of claims 1-8 and 12-16 over *Wieczorek* in view of *Nakajyo* and in further view of *Yamamoto*. The Applicant respectfully submits that claims 1-8 and 12-16 as listed herein fully satisfy the requirements of 35 U.S.C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested. If any points remain in issue that may best be resolved through a personal or telephonic interview, Examiner Reis is respectfully requested to contact the undersigned at the telephone number listed below.

Dated: **February 24, 2005**

Respectfully submitted,
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